and expandable graphics system by allowing the memory controller to accommodate a plurality of interfaces such as graphics interface and interface controller.

7. As per claims 2-3 and 8-9, Fisher et al disclosed a dedicated bus interface coupling to the graphics controller to the memory controller hub (Fig. 1, Item No. 22).

Applicant disagrees.

Applicant has invented a memory controller hub having an internal graphics subsystem and a cache that is adapted to store addresses of locations in physical memory, which are available to the internal graphics subsystem for storing graphics data and which are available to an external graphics controller coupled to the memory controller hub to store graphics data. Thus, the same cache is used for storing physical memory addresses available for use by an internal graphics subsystem and for storing physical memory addresses available for use by an external graphics controller. As explained in the applicant's specification, the cache may be used to store Graphics Address Remapping Table (GART) entries (used by the external graphics controller in AGP mode) or Graphics Translation Table (GTT) entries (used by the internal graphics subsystem in Gfx mode). GART and GTT entries are used for translating virtual memory addresses into physical memory addresses. The specification explains an advantage of having a single cache that can store both GART and GTT entries: "Since the number of GART entries or GTT entries that may be stored in TLB 28 is limited by the physical die area size of the TLB, using the same TLB to store GART entries in AGP mode and to store GTT entries in Gfx mode effectively doubles the number of GART or GTT entries that may be stored in TLB compared to the number that could be stored if separate TLBs were used for GART and GTT entries." Specification at 9-10.

Fisher does not substantially disclose the claimed invention.

First, although Fisher mentions in the "Background of the Invention" section that "texture mapping hardware subsystems typically include a local memory cache that stores texture mapping data associated with the portion of the object being rendered," col. 1:58-61, Fisher provides no teaching or suggestion that this cache is included in a memory controller hub. The cache is mentioned only once in the "Background" section but is never mentioned again and is not connected to a memory controller hub in any way. Thus, Fisher does not disclose or suggest a "memory controller hub comprising . . . a cache . . . ."

Second, unlike the claimed invention, the "local memory cache" mentioned by Fisher is not "adapted to store addresses of locations in physical memory." Rather, Fisher's cache is used to "store[] texture mapping data associated with the portion of the object being rendered." Thus, Fisher's cache is used to store graphics data themselves, unlike the cache in the claimed invention, in which a cache is used to store addresses of physical memory locations available for storing graphics data.

Third, Fisher does not disclose a memory controller hub having an internal graphics subsystem.

Ajanovic does not remedy the deficiencies of Fisher. Ajanovic does not disclose or suggest a memory controller hub comprising a cache, nor does Ajanovic disclose or suggest "a cache adapted to store addresses of locations in physical memory available to the internal graphics subsystem for storing graphics data and available to an external graphics controller coupled to the memory controller hub to store graphics data." Additionally, applicant disagrees with the Examiner when the Examiner states that "Ajanovic et al disclosed a memory controller which includes an internal graphics subsystem adapted to perform graphics operations on data (Fig. Items No. 110, 113, col 3, lines 45-47)." Ajanovic discloses a memory controller hub 110 that includes a graphics interface 113 (col. 3:45-53 and Fig. 1). However, the graphics interface 113 is not adapted to perform graphics operations on data. Rather, graphics interface 113 is coupled to a graphics accelerator 130 and is used to communicate data from the memory controller hub 110 to the graphics accelerator 130, so that the graphics accelerator can perform graphics operations on the data. However, the graphics accelerator is outside the memory controller hub, and the memory controller hub does not include the graphics accelerator.

Independent claims 1, 7, and 13 are allowable for at least the foregoing reasons. Claims 2-3 depend from claim 1 and are allowable at least for the same reasons that the claims 1 is allowable. Claims 8-9 depend from claim 7 and are allowable at least for the same reasons that the claims 7 is allowable.

8. Claims 4-6, 10-12 and 14-16 are rejected under 35 U. S. C. 103(a)as being unpatentable over Fisher et al in view of Ajanovic et al as applied to claims 1-3, 7-9 and 13 above, further in view of Surti et al (US Patent No. 6,496,193).

9. Surti was cited in the last office action.

10. As per claims 4-6, 10-12 and 14-16, Fisher et al tirther disclose a cache adapted to store addresses of locations in physical memory (col. 1, lines 58-61), but Fisher et al and Ajanovic et al did not explicitly disclose that the memory controller hub is configured to provide a block of linear, virtual memory address by graphics subsystem or graphics controller. However, Surti et al disclosed a method and apparatus for fast loading of texture data into a tile memory, wherein texture data are store in system memory in a tile format that allows an entire cache tile to be stored linearly in memory space (col. 2, lines 8-10; col. 4, lines 3-5, 47-51). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would not only allow the graphics engine to access memory faster without causing an excessive number of page misses in the memory subsystem; but also allow the graphics engine to take advantage of the high burst rate fills to load the cache, thereby enhance the processing speed of the system.

Claims 4-6 depend from claim 1 and are allowable for at least the same reasons that claim 1 is allowable. Claims 10-12 depend from claim 7 and are allowable for at least the same reasons that claim 7 is allowable. Claims 14-16 depend from claim 13 and are allowable for at least the same reasons that claim 13 is allowable.

11. Applicant's arguments with respect to claims 11-16 have been considered but are moot in view of the new ground(s) of rejection.

12. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension policy as set forth in 37 CFR 1.136(a).

Applicant submits that the Office has improperly made this action final, because the Examiner introduced at least one new ground of rejection that was neither necessitated by applicant's amendment nor based on information submitted in an information disclosure statement. Applicant's previous amendment merely highlighted what was already apparent from the original claim – that the memory controller hub itself includes a graphics subsystem and is coupled to a graphics controller. Because the memory controller hub includes a graphics subsystem, that graphics subsystem is an internal graphics subsystem to the memory controller hub. Similarly, because the memory controller hub is coupled to a graphics controller, the graphics controller to which the hub is coupled is an external graphics controller to the hub. Applicants amendment did not necessitate the Examiner's admitted "new ground(s) of rejection." Accordingly, the rejection has been made final improperly.

Applicant requests that the finality of this rejection be removed.

Applicant asks that all claims be allowed in view of the foregoing remarks.

No fees are believed to be due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050, referencing Attorney Docket No. 10559-165001.

Respectfully submitted,

Date: 8/11/03

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